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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/603,990	06/26/2003	Mi-Sook Nam	053785-5120	3882
9629 7590 04/02/2009 MORGAN LEWIS & BOCKIUS LLP 1111 PENNSYLVANIA AVENUE NW WASHINGTON, DC 20004				
EXAMINER				
SCHECHTER, ANDREW M				
ART UNIT		PAPER NUMBER		
2871				
MAIL DATE		DELIVERY MODE		
04/02/2009		PAPER		

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

### Office Action Summary

**Application No.**

10/603,990

**Applicant(s)**

NAM, ET AL.

**Examiner**

ANDREW SCHECHTER

**Art Unit**

2871

**Period for Reply** -- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 24 February 2009.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-5, 8-15 and 17-21 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-5, 8-15 and 17-21 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 26 June 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_\_

## **DETAILED ACTION**

### ***Request for Continued Examination***

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 2 February 2009 has been entered.

### ***Response to Arguments***

2. Applicant's arguments filed 2 February 2009 have been fully considered but they are not persuasive. Applicant's arguments have been considered but are moot in view of the new ground(s) of rejection.

The applicant has amended the independent claims to recite "the reflective layer not overlapping the thin film transistor", and argues [p. 11] that none of the cited references teaches or suggests this feature. This is not persuasive for the reasons discussed below.

The applicant quotes the examiner as stating on p. 2 of the last office action that "Mitsui's reflective layer does not overlap the TFT", which is not correct, nor would it be helpful to the applicant's position. (Presumably the "not" in the quote was a typographical error.) What the examiner actually stated was that, given a particular

definition of the extent of a TFT, "the examiner would agree that *Mitsui's* reflective layer does overlap the TFT, so defined." That definition was problematic, however, for reasons discussed in that paragraph, and the applicant's response did not address whether they are willing to accept that definition or not. As the examiner stated in the Advisory Action of 11 February 2009, there is not a generally held definition for the region defined by a TFT (that the examiner is aware of). In the Advisory Action, the examiner offered several possible definitions, which the applicant has so far not addressed. Since the point of novelty rests on whether the reflective layer overlaps the TFT, there must be an agreed upon definition or understanding of the spatial extent of a TFT in the prior art devices, otherwise the metes and bounds of the claims are not made clear.

Since this issue has not been resolved, the claims are rejected below as unclear under 35 USC 112, 2nd paragraph. For examining purposes a definition is assumed under which the following prior art rejections are also appropriate.

### ***Claim Rejections - 35 USC § 112***

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1-5, 8-15, and 17-21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The claims recite "the reflective layer not overlapping the thin film transistor" or the equivalent. This is unclear. How does the applicant define the extent of the TFT, so that it is clear whether it is overlapped by the reflective layer? Claim 1 recites the TFT including a gate electrode, an active layer, and source and drain electrodes, but the extent of these is undefined; for instance, the gate electrode would not include the gate line, and the active layer would not include a part of the active layer which was contiguous with the rest of the active layer but far from the gate electrode and channel region.

The examiner suggests that the simplest and least-problematic definition of the extent in plan view of a TFT would be the channel region, where the gate electrode and active layer overlap and which is either bordered or overlapped by the source and drain electrodes. The components of the TFT would be the parts of the gate electrode, active layer, source electrode, and drain electrode which overlap or border that region. The remaining parts of the gate wiring and source/drain wiring carry signals to and from the TFT, but are not part of the TFT itself. Assuming this definition, the reflective layer in *Mitsui* does not overlap the TFT, so the previous prior art rejections are maintained.

Since *Mitsui* expressly teaches that the reflective should not overlap at least the channel region of the TFT, the critical difference between the present invention and that of *Kubota* in view of *Mitsui* may actually be the overlap or connection between the reflective layer and the electrode extending from the drain of the TFT, rather than the reflective layer overlapping the TFT per se.

The examiner notes that he is available to discuss these issues if the applicant feels that would be helpful to bring this case to a resolution.

***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 1-3, 10, 12, 13, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Kubota, et al.*, US 2002/0171792 in view of *Mitsui et al.*, U.S. Patent No. 5,408,345, in view of *Maeda et al.*, U.S. Patent No. 7,123,325 and further in view of official notice/admitted prior art.

*Kubota* discloses [see Fig. 1, for instance] a transfective liquid crystal display device comprising a substrate [2] having a reflective portion and a transmissive portion, a gate line [14a] on the substrate, a data line [17], a thin film transistor [14] connected to the gate line and the data line, and including a gate electrode [14a], an active layer [12], and source and drain electrodes [14b, 14c]; an insulating layer [19] having an open portion at the transmissive portion, a reflective layer [20] on the insulating layer having a transmissive hole at the open portion, a pixel electrode [3] on the reflective layer, an opposing substrate [5] facing the substrate, and a common electrode [6] on an inner surface of the opposing substrate, the common electrode being substantially flat.

*Kubota* possibly does not explicitly disclose that the gate and data lines cross to form a pixel region; the examiner takes official notice that this was well-known in the art at the time of the invention [as this was not traversed by the applicant, this is considered admitted prior art; see MPEP 2144.03]. It would have been obvious to one of ordinary skill in the art at the time of the invention to have it so, motivated by the desire to form the standard active matrix of pixels for the display.

*Kubota* does not disclose the reflective layer not overlapping the thin film transistor. However, *Mitsui* discloses [see Fig. 5] an analogous device having the analogous reflective layer [38] not overlapping [see above discussion under 35 USC 112, 2<sup>nd</sup> paragraph] the thin film transistor [40], and teaches doing so [col. 3, lines 32-45], saying that when the reflective layer does overlap the TFT, the signal applied to the reflective layer can spuriously act as a gate electrode, causing the TFT to malfunction, and can produce an undesirable parasitic capacitance between the reflective layer and the gate electrode. It would have been obvious to one of ordinary skill in the art at the time of the invention to have the reflective layer not overlapping the TFT, motivated by the desire to avoid such electrical problems as taught by *Mitsui*.

*Kubota* does not disclose that the insulating layer [19] has a plurality of uneven patterns consisting of a first organic material layer within the reflective portion, the uneven patterns partially covering the substrate, and a second organic material layer on the first organic material layer. *Maeda* [see Fig. 10K, for instance] discloses an analogous transfective LCD in which the insulating layer under the reflective layer and pixel electrode has a plurality of uneven patterns consisting of a first organic material

layer [51] within the reflective portion, the uneven patterns partially covering the substrate, and a second organic material layer [52] on the first organic material layer. It would have been obvious to one of ordinary skill in the art at the time of the invention to have it be so, motivated by the desire to make the surface of the reflective layer bumpy, so that the light diffusively reflects off the surface (rather than reflecting like a mirror), thus improving the display quality. Claim 1 is therefore unpatentable.

Considering the additional limitations of claim 10, *Kubota* also discloses a liquid crystal layer between the pixel electrode, wherein the pixel electrode and the common electrode are separated by a first cell gap in the transmissive portion, and a second cell gap in the reflective portion, and the first cell gap is twice greater than the second cell gap [see paragraph 0084, for instance]. Claim 10 is therefore unpatentable as well.

Considering the additional limitations of claims 12 and 19, *Kubota* in view of *Maeda* also discloses the method of fabricating the above LCD, except perhaps for the step of performing an exposure and development process on the first and second photosensitive organic material layers. *Maeda* discloses using organic layers which are photosensitive, but does not necessarily disclose the particular patterning steps recited. The examiner takes official notice that for patterning such organic layers, performing an exposure and development process on organic layers was well known [as this was not traversed by the applicant, this is considered admitted prior art; see MPEP 2144.03]. It would have been obvious to one of ordinary skill in the art at the time of the invention to do so, motivated by this being the standard technique for patterning organic materials in the art. Claims 12 and 19 are therefore unpatentable as well.



The first and second organic material layers are formed from a photosensitive material, including comprising a photo-acrylic resin [see *Maeda*, col. 13, lines 29-35, for instance], so claims 2 and 3 are also unpatentable. Considering claim 13, it would have been "obvious to try" a photo-acrylic resin for both the first and second photosensitive material layers, with predictable results, as this type of material is routinely used in forming such organic layers, as evidenced by *Maeda* above, so claim 13 is also unpatentable.

7. Claims 4, 5, 14, 15, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Kubota, et al.*, US 2002/0171792, *Mitsui et al.*, U.S. Patent No. 5,408,345, *Maeda et al.*, U.S. Patent No. 7,123,325, and official notice/admitted prior art as applied above, and further in view of *You*, U.S. Patent No. 7,023,508.

*Kubota* discloses an insulating layer [18] covering the gate line, the data line, and the thin film transistor, but does not state that it is inorganic. *You* discloses an analogous device [see Fig. 3, for instance], which has an inorganic material layer [116] made of silicon nitride, covering the gate line, the data line, and the thin film transistor. It would have been obvious to one of ordinary skill in the art at the time of the invention to use an inorganic layer, such as *You*'s silicon nitride, in the above device, motivated by *You*'s teaching that this maintains the reliability of the transistor and pads and enhances the strength of COG bonding [col. 9, lines 1-8]. Claims 4, 5, 14, 15, and 21 are therefore unpatentable.

8. Claims 8, 9, 11, 17, 18, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Kubota, et al.*, US 2002/0171792, *Mitsui et al.*, U.S. Patent No.

5,408,345, *Maeda et al.*, U.S. Patent No. 7,123,325, and official notice/admitted prior art as applied above, in view of official notice.

*Kubota* does not necessarily disclose gate pads, data pads, or a capacitor electrode overlapping the gate line. The examiner takes official notice that these features are well-known and conventional in the art [as this was not traversed by the applicant, this is considered admitted prior art; see MPEP 2144.03]. It would have been obvious to one of ordinary skill in the art at the time of the invention to include them in the above device, motivated by the desire to make electrical contact to the gate and data lines, and to provide a reliable storage capacitance to improve the display quality. Claims 8 and 17 are therefore unpatentable.

Similarly, to make electrical contact to these, it is necessary to have drain contact holes, capacitor contact holes, gate pad contact holes, and data pad contact holes as recited; the examiner takes official notice that such are well-known [as this was not traversed by the applicant, this is considered admitted prior art; see MPEP 2144.03] and would have been obvious to one of ordinary skill in the art at the time of the invention, for the purpose of making electrical contact to the relevant electrodes through the second organic material layer. Claims 9 and 18 are therefore unpatentable.

The difference in cell gaps is provided by the height of the insulating film, and for the first (transmissive) cell gap to be twice the second (reflective) cell gap, the height needs to be equal to the second cell gap. The uneven patterns are equal to or less than this height, so they have a height equal to or less than the second cell gap, as required by claims 11 and 20. Claims 11 and 20 are therefore unpatentable. Even were this not

true, adjusting the height of the uneven patterns to improve the reflective properties of the reflective layer, or to optimize the relative cell gaps for better liquid crystal behavior, would have been obvious to one of ordinary skill in the art at the time of the invention, motivated by the desire to optimize these features of the device, so claims 11 and 20 are unpatentable.

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew Schechter whose telephone number is (571) 272-2302. The examiner can normally be reached on Monday - Friday, 9:00 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Andrew Schechter/  
Primary Examiner, Art Unit 2871  
Technology Center 2800  
30 March 2009